# Flexible Transformer Based Multilevel Inverter Topologies

Amin Ashraf Gandomi[1, *], Saeid Saeidabadi[1], Seyed Hossein Hosseini[1, 2], Ebrahim Babaei[1], Yasser Ashraf Gandomi[3]

[1] Faculty of Electrical & Computer Engineering, University of Tabriz, Tabriz, Iran
[2] Engineering Faculty, Near East University, 99138 Nicosia, North Cyprus, Mersin 10, Turkey
[3] Department of Mechanical, Aerospace and Biomedical Engineering, University of Tennessee, Knoxville, Tennessee 37996, USA
[*] aashrafg@gmail.com

**Abstract: Cascaded multilevel inverters have been proposed that utilize transformers in the basic unit. The proposed inverters primarily serve to step up the input voltages in addition to using lower number of components in comparison to traditional multilevel inverters In order to generate all voltage levels (even and odd) at the output, three different algorithms are proposed to determine the magnitude of DC voltage sources and transformer turn ratios. Also, the basic inverter unit was further developed and two new flexible MLI structures have been obtained. The developed structures increase the input voltage with no need for an additional boost converter. Reduction in the number of power switches, the peak inverse voltage (PIV) and the number of DC voltage sources are other advantages of the proposed topologies. Also, a simple cost model was developed and the dimensionless cost coefficient was determined. The overall cost of the proposed MLIs was compared to the similar MLIs from the literature. It was shown that the proposed MLI decrease overall cost of system if the cost coefficient is selected appropriately. To verify the performance of proposed topologies simulated by the mathematical model; several lab-scale inverters were built and tested and good agreement was achieved.**

## 1. Introduction

The renewable energy sources such as wind, solar and tidal energy in the form of hybrid energy systems are being integrated into the national energy grid via utilizing the grid-scale energy storage systems [1]. The hybrid systems usually include a variety of energy generation sources (e.g. photovoltaic (PV) and wind turbines) and energy storage devices (e.g. redox flow batteries) [2-4]. The schematic of the hybrid energy system has been shown in Fig. 1. One of the main components of the hybrid energy systems is the DC/AC power conversions as inverters. Several inverter topologies have been proposed that the multilevel inverters (MLIs) are among the most frequently used ones.

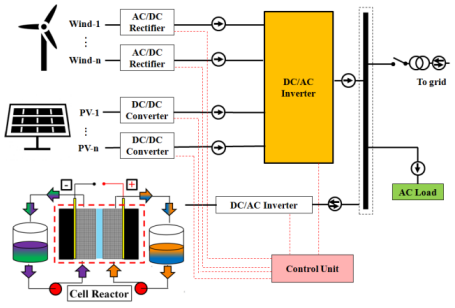


***Fig. 1.*** *Sample graph with blue (dotted), green (solid) and red (dashed) lines*

The application of the MLIs results in some unique features such as the operation in high power and medium voltage ranges, the generation of the high quality output voltage with low total harmonic distortion (THD) and lower standing voltage on switches [5, 6]. These superior properties have increased the application of the MLIs in hybrid energy systems as well as some other industries such as motor drives, flexible AC transmission systems (FACTS), electric vehicles, and many others [7, 8]. Three main types of the MLIs are diode clamped multilevel inverters (DCMLIs), flying capacitor multilevel inverters (FCMLIs) and cascaded multilevel inverters (CMLIs) [9]. In the DCMLIs, the desired output voltage is being generated through a combination of the voltage of capacitors connected in series. Beside large number of diodes that are used in DCMLIs, this type also suffers from non-uniformity of the voltage stresses on the clamped diodes, necessitating the application of the diodes with different ratings [10].

In FCMLIs configuration, there is no clamping diode and the output voltage is formed by combining the voltage of floating capacitors. Also in this type, to generate higher number of voltage levels, large number of flying capacitors are needed, which complicates the control strategy and the voltage balancing process [11-14].

The CMLIs are available in different types but the simplest form is the cascaded H-bridge (CHB) topology [15]. Relatively simple and modular structure has increased the application of this configuration. Also for this type, the voltage balancing of the capacitors is not cumbersome.

The MLIs can also be categorized as symmetric (equal input DC sources) and asymmetric (unequal input DC sources) structures [16]. In [17-23], different symmetric cascaded multilevel inverters have been presented. The main advantage of the symmetric inverters is the decreased number of different voltage magnitudes applied on the DC sources. However, they require large number of components and DC sources [26]. In order to increase the number of output voltage levels with lower number of power semiconductor devices, different asymmetric multilevel

inverters along with different algorithms to determine the magnitudes of DC voltage sources have been presented [24-29]. In [24, 25] two cascaded multilevel inverters have been introduced that although the number of gate drivers have been decreased in these topologies; but the number of insulated gate bipolar transistors (IGBTs) and the overall cost has been increased since the bidirectional power switches have been utilized. In [26, 27], two new MLIs have been presented that in comparison to the previous topologies, requires lower number of DC voltage sources and power switches, but increases the variety of DC voltage sources and PIV of the switches. Different algorithms for determining the value of the input DC voltage sources with an attempt of increasing the number of output voltage levels have already been developed for some of the CMLIs discussed earlier. Also, the capability of the CMLIs operations under the symmetric and asymmetric DC voltage sources has already been demonstrated [28, 29]. The results presented in [16-29] demonstrate that the asymmetric cascaded H-bridge multilevel inverters generate high quality voltage waveform with lower THD utilizing the same number of DC voltage sources, in comparison to the symmetric topology. To increase the number of output voltage levels, multilevel inverters with coupled inductors have been presented that utilizes lower number of switches and DC sources in comparison to conventional cascaded H-bridge multilevel inverters [30, 31]. Along with different types and configurations, several switching patterns have also been proposed for the MLIs. The most common switching algorithms are sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE), and space vector modulation (SVM) [32-34].

In this paper, new topologies with symmetric and asymmetric configurations have been proposed for MLIs. Several algorithms for determining the magnitude of DC sources and turn ratio of the transformers is also proposed. The new topologies developed throughout this work have been implemented with the main idea of generating the multilevel voltages with higher gain while utilizing the minimum number of power electronic devices. These properties, all together, making the proposed inverters a potential device to be used in the renewable energy applications. In order to verify the validity of the proposed topology; lab-scale prototypes have been designed and built and the data have been compared to some previously established topologies.

## 2. The proposed inverters structures

The basic structure of the proposed multilevel inverters is shown in Fig. 2. In this structure, transformer is used for two main reasons. First, by using the transformer in the proposed inverter, this structure can produce more number of output voltage levels with lower number of switches and DC sources. Second, due to transformer's turn ratios in this structure, output voltage gain is more than one that is one of the main merits of this structure. According to transformer turn ratio ($\frac{n_1}{n_2}$), the basic unit can generate 7-level voltage with unequal steps ($(1+\frac{n_1}{n_2})V_{in}$, $\frac{n_1}{n_2}V_{in}$, $V_{in}$, $0$, $-V_{in}$, $-\frac{n_1}{n_2}V_{in}$, $-(1+\frac{n_1}{n_2})V_{in}$) with input DC voltage of $V_{in}$ [35]. The switching pattern for the basic unit is as Table 1.

By adding the output voltage before the transformer and voltage across the primary winding of transformer, the output unequal seven-level voltage in basic unit is produced. Average voltage of the primary winding of transformer in the proposed inverter is calculated as follow:

$$V_{ave}=\frac{1}{T}\int_0^{t_1}0dt+\int_{t_1}^{\frac{T}{2}-t_1}\frac{n_1}{n_2}V_{in}dt+\int_{\frac{T}{2}}^{\frac{T}{2}+t_1}0dt+\int_{\frac{T}{2}+t_1}^{T-t_1}-\frac{n_1}{n_2}V_{in}dt=0 \quad (1)$$

According to (1), the average value of primary voltage of transformer is zero. Therefore, there is not saturation problem in the basic unit.

**Table 1** Switching states in the basic unit

| Inverter Output Voltage | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
|---|---|---|---|---|---|---|
| $(\frac{n_1}{n_2}+1)V_{in}$ | on | off | on | off | off | on |
| $\frac{n_1}{n_2}V_{in}$ | off | on | on | off | off | on |
| $V_{in}$ | on | off | off | on | off | on |
| | off | on | off | on | off | on |
| $0$ | on | off | on | off | on | off |
| $-V_{in}$ | off | on | on | off | on | off |
| $-\frac{n_1}{n_2}V_{in}$ | on | off | off | on | on | off |
| $-(\frac{n_1}{n_2}+1)V_{in}$ | off | on | off | on | on | off |

In order to increase the number of output voltage levels, the basic unit shown in Fig. 2 was further improved based on the cascaded units, transformer and input voltage source.

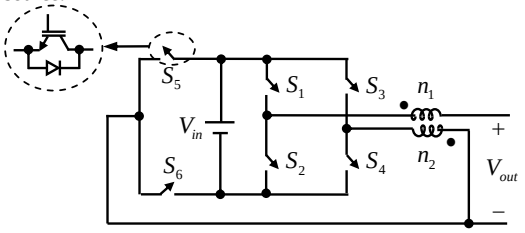


***Fig. 2.*** *Basic unit of the proposed multilevel inverters*

### 2.1. Cascaded multilevel inverter

The single-phase cascaded multilevel inverter proposed in this work consists of $n$ modules connected in series (Fig. 3). Three different algorithms are implemented for the inverter to determine the values of DC voltage sources and transformers' turn ratio. The generation of the maximum number of voltage levels (even and odd output levels) was the main design criteria within the various algorithms.

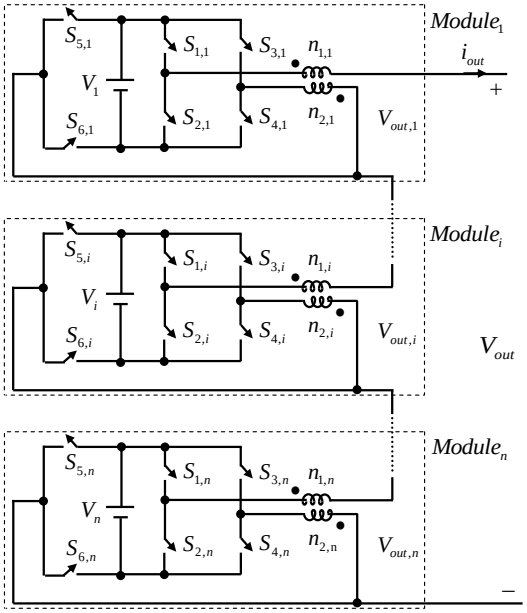


***Fig. 3.*** *The proposed cascaded multilevel inverter*

*2.1.1 First algorithm, symmetric cascaded structure (P1):* In this algorithm, the magnitudes of the input voltage sources as well as the turn ratio of the transformers are kept unchanged. The magnitude of the input voltage sources ($V_i$) and the turn ratios ($\frac{n_{1,i}}{n_{2,i}}$) of the transformers in $i^{th}$ basic unit are applied as the following:

$$V_i = V_{in} \quad for \quad i = 1,2,...,n \quad (2)$$

$$\frac{n_{1,i}}{n_{2,i}} = \frac{2}{1} \quad for \quad i = 1,2,...,n \quad (3)$$

The application of the new algorithm for the cascaded *n*-module inverter enables generating all the negative and positive voltage levels from 0 to $(3n)V_{in}$ with the steps of $V_{in}$. In this case, the switch-rate ($R_s$), is calculated according to (4). Here, $V_{stress}$ and $I_{stress}$ represent the voltage and current stress levels of the switch, respectively.

$$R_s = V_{stress} \times I_{stress} \quad (4)$$

According to (4), for the different switches, the following equations are used to calculate the voltage stress, current stress and rating of the switches.

$$(S_{1,i}, S_{2,i}): \begin{cases} V_{stress} = V_{in} \\ I_{stress} = I_{out} \\ R_s = V_{in} \times I_{out} \end{cases} ,i = 1,2,...,n \quad (5)$$

$$(S_{3,i}, S_{4,i}): \begin{cases} V_{stress} = V_{in} \\ I_{stress} = 2I_{out} \\ R_s = 2V_{in} \times I_{out} \end{cases} ,i = 1,2,...,n \quad (6)$$

$$(S_{5,i}, S_{6,i}): \begin{cases} V_{stress} = V_{in} \\ I_{stress} = 3I_{out} \\ R_s = 3V_{in} \times I_{out} \end{cases} ,i = 1,2,...,n \quad (7)$$

*2.1.2 Second algorithm, asymmetric cascaded (P2):* In this algorithm, the values of the input voltage source are not equal but, the transformers' turn ratios are similar. The input voltage sources and turn ratios of the transformers are:

$$V_i = 7^{i-1} V_{in} \quad for \quad i = 1,2,...,n \quad (8)$$

$$\frac{n_{1,i}}{n_{2,i}} = \frac{2}{1} \quad for \quad i = 1,2,...,n \quad (9)$$

This algorithm assures that the proposed cascaded *n*-module inverter generates all the negative and positive voltage levels from 0 to $(\frac{7^n - 1}{2})V_{in}$. The voltage stress, current stress and rating of the switches are calculated according to the following equations.

$$(S_{1,i}, S_{2,i}): \begin{cases} V_{stress} = 7^{i-1} V_{in} \\ I_{stress} = I_{out} \\ R_s = 7^{i-1} V_{in} \times I_{out} \end{cases} ,i = 1,2,...,n \quad (10)$$

$$(S_{3,i}, S_{4,i}): \begin{cases} V_{stress} = 7^{i-1} V_{in} \\ I_{stress} = 2I_{out} \\ R_s = 2 \times 7^{i-1} \times V_{in} \times I_{out} \end{cases} ,i = 1,2,...,n \quad (11)$$

$$(S_{5,i}, S_{6,i}): \begin{cases} V_{stress} = 7^{i-1} V_{in} \\ I_{stress} = 3I_{out} \\ R_s = 3 \times 7^{i-1} \times V_{in} \times I_{out} \end{cases} ,i = 1,2,...,n \quad (12)$$

*2.1.3 Third algorithm, symmetric cascaded structure (P3):* In this mode, the values of the input voltage sources are kept constant with varying the transformers' turn ratios. The input voltage sources and turn ratios of the transformers are calculated as the following:

$$V_i = V_{in} \quad for \quad i = 1,2,...,n \quad (13)$$

$$\frac{n_{1,i}}{n_{2,i}} = \frac{(3^i - 1)}{1} \quad for \quad i = 1,2,...,n \quad (14)$$

As a result, the proposed cascaded n-module inverter generates all the negative and positive voltage levels from 0 to $\frac{(3^{n+1} - 3)}{2}V_{in}$. The voltage stress, current stress and rating of the switches are obtained using the following formulas.

$$(S_{1,i},S_{2,i}):\begin{cases}V_{stress}=V_{in}\\ I_{stress}=I_{out}\\ R_s=V_{in}\times I_{out}\end{cases},i=1,2,...,n \quad (15)$$

$$(S_{3,i},S_{4,i}):\begin{cases}V_{stress}=V_{in}\\ I_{stress}=(3^i-1)I_{out}\\ R_s=(3^i-1)\times V_{in}\times I_{out}\end{cases},i=1,2,...,n \quad (16)$$

$$(S_{5,i},S_{6,i}):\begin{cases}V_{stress}=V_{in}\\ I_{stress}=3^i\times I_{out}\\ R_s=3^i\times V_{in}\times I_{out}\end{cases},i=1,2,...,n \quad (17)$$

The switching states for the three proposed algorithms are shown in Table 2 ($n=2$).

### 2.2. Multilevel inverter developed from transformer ($P_4$)

The addition of two unidirectional power electronic switches and one low frequency transformer to the basic unit in each step, results in a new flexible topology for the multilevel inverter as depicted in Fig. 4.

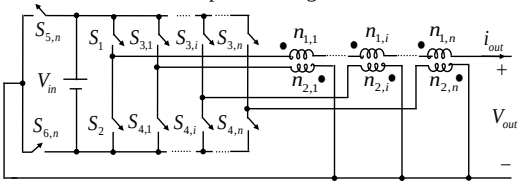


***Fig. 4.*** *The proposed multilevel inverter developed from transformers*

In this structure, the main objective is to generate the maximum output voltage levels (all the even and odd); therefore, the following algorithm is implemented to determine the turn ratios.

$$\frac{n_{1,i}}{n_{2,i}}=\frac{2^i}{1} \quad for \quad i=1,2,...,n \quad (18)$$

All the negative and positive voltage levels from $0$ to $(2^{n+1}-1)V_{in}$ are producible through the application of the new algorithm. The switching states in this structure are shown in Table 3.

**Table 2** Switching states in the proposed cascaded inverter for the positive output voltage levels ($n=2$)

| $v_o$ | $S_{1,1}$, $\overline{S_{2,1}}$ | $S_{3,1}$, $\overline{S_{4,1}}$ | $S_{5,1}$, $\overline{S_{6,1}}$ | $S_{1,2}$, $\overline{S_{2,2}}$ | $S_{3,2}$, $\overline{S_{4,2}}$ | $S_{5,2}$, $\overline{S_{6,2}}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $V_1$ | 1 | 0 | 0 | 0 | 0 | 0 |
| $\frac{n_{1,1}}{n_{2,1}}V_1$ | 0 | 1 | 0 | 0 | 0 | 0 |
| $(1+\frac{n_{1,1}}{n_{2,1}})V_1$ | 1 | 1 | 0 | 0 | 0 | 0 |
| $V_2-(1+\frac{n_{1,1}}{n_{2,1}})V_1$ | 0 | 0 | 1 | 1 | 0 | 0 |
| $V_2-\frac{n_{1,1}}{n_{2,1}}V_1$ | 1 | 0 | 1 | 1 | 0 | 0 |
| $V_2-V_1$ | 0 | 1 | 1 | 1 | 0 | 0 |
| $V_2$ | 0 | 0 | 0 | 1 | 0 | 0 |
| $V_1+V_2$ | 1 | 0 | 0 | 1 | 0 | 0 |
| $\frac{n_{1,1}}{n_{2,1}}V_1+V_2$ | 0 | 1 | 0 | 1 | 0 | 0 |
| $(1+\frac{n_{1,1}}{n_{2,1}})V_1+V_2$ | 1 | 1 | 0 | 1 | 0 | 0 |
| $\frac{n_{1,2}}{n_{2,2}}V_2-(1+\frac{n_{1,1}}{n_{2,1}})V_1$ | 0 | 0 | 1 | 0 | 1 | 0 |
| $\frac{n_{1,2}}{n_{2,2}}V_2-\frac{n_{1,1}}{n_{2,1}}V_1$ | 1 | 0 | 1 | 0 | 1 | 0 |
| $\frac{n_{1,2}}{n_{2,2}}V_2-V_1$ | 0 | 1 | 1 | 0 | 1 | 0 |
| $\frac{n_{1,2}}{n_{2,2}}V_2$ | 0 | 0 | 0 | 0 | 1 | 0 |
| $V_1+\frac{n_{1,2}}{n_{2,2}}V_2$ | 1 | 0 | 0 | 0 | 1 | 0 |
| $\frac{n_{1,1}}{n_{2,1}}V_1+\frac{n_{1,2}}{n_{2,2}}V_2$ | 0 | 1 | 0 | 0 | 1 | 0 |
| $(1+\frac{n_{1,1}}{n_{2,1}})V_1+\frac{n_{1,2}}{n_{2,2}}V_2$ | 1 | 1 | 0 | 0 | 1 | 0 |
| $(1+\frac{n_{1,2}}{n_{2,2}})V_2-(1+\frac{n_{1,1}}{n_{2,1}})V_1$ | 0 | 0 | 1 | 1 | 1 | 0 |
| $(1+\frac{n_{1,2}}{n_{2,2}})V_2-\frac{n_{1,1}}{n_{2,1}}V_1$ | 1 | 0 | 1 | 1 | 1 | 0 |
| $(1+\frac{n_{1,2}}{n_{2,2}})V_2-V_1$ | 0 | 1 | 1 | 1 | 1 | 0 |
| $(1+\frac{n_{1,2}}{n_{2,2}})V_2$ | 0 | 0 | 0 | 1 | 1 | 0 |
| $V_1+(1+\frac{n_{1,2}}{n_{2,2}})V_2$ | 1 | 0 | 0 | 1 | 1 | 0 |
| $\frac{n_{1,1}}{n_{2,1}}V_1+(1+\frac{n_{1,2}}{n_{2,2}})V_2$ | 0 | 1 | 0 | 1 | 1 | 0 |
| $(1+\frac{n_{1,1}}{n_{2,1}})V_1+(1+\frac{n_{1,2}}{n_{2,2}})V_2$ | 1 | 1 | 0 | 1 | 1 | 0 |

Similar to previous cases, the following equations (19-21) are utilized to calculate the voltage stress, current stress and rating of the switches.

$$(S_1,S_2):\begin{cases}V_{stress}=V_{in}\\ I_{stress}=I_{out}\\ R_s=V_{in}\times I_{out}\end{cases} \quad (19)$$

$$(S_{3,i},S_{4,i}):\begin{cases}V_{stress}=V_{in}\\ I_{stress}=2^i I_{out}\\ R_s=2^i\times V_{in}\times I_{out}\end{cases},i=1,2,...,n \quad (20)$$

$$(S_5,S_6):\begin{cases}V_{stress}=V_{in}\\ I_{stress}=(2^{n+1}-1)I_{out}\\ R_s=(2^{n+1}-1)\times V_{in}\times I_{out}\end{cases} \quad (21)$$

**Table 3** Switching states in the proposed inverter developed from transformer for the positive output voltage levels ($n=2$)

| $v_o$ | $S_1/\overline{S_2}$ | $S_{3,1}/\overline{S_{4,1}}$ | $S_{3,2}/\overline{S_{4,2}}$ | $S_5/\overline{S_6}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| $V_1$ | 1 | 0 | 0 | 0 |
| $\frac{n_{1,1}}{n_{2,1}}V_1$ | 0 | 1 | 0 | 0 |
| $(1+\frac{n_{1,1}}{n_{2,1}})V_1$ | 1 | 1 | 0 | 0 |
| $\frac{n_{1,2}}{n_{2,2}}V_1$ | 0 | 0 | 1 | 0 |
| $V_1+\frac{n_{1,2}}{n_{2,2}}V_1$ | 1 | 0 | 1 | 0 |
| $\frac{n_{1,1}}{n_{2,1}}V_1+\frac{n_{1,2}}{n_{2,2}}V_1$ | 0 | 1 | 1 | 0 |
| $(1+\frac{n_{1,1}}{n_{2,1}})V_1+\frac{n_{1,2}}{n_{2,2}}V_1$ | 1 | 1 | 1 | 0 |

### 2.3. Multilevel inverter developed from transformer ($P_5$)

The addition of two extra unidirectional power electronic switches and one DC source to the basic unit in each step results in a new configuration of multilevel inverter (Fig. 5) which is a flexible topology similar to the configuration $P_4$.

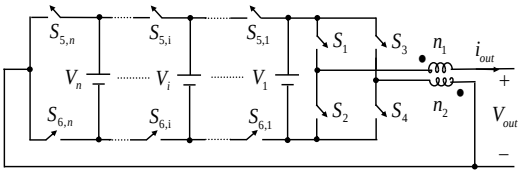


***Fig. 5.*** *The proposed multilevel inverter developed from input voltage sources*

In order to achieve the maximum number of even and odd output levels, the following algorithm is utilized to determine the magnitude of the input voltage sources and turn ratios.

$$V_i=(\frac{2^{i+1}-1}{3})V_{in} \quad for \quad i=1,2,...,n \quad (22)$$

$$\frac{n_1}{n_2}=\frac{2}{1} \quad (23)$$

This algorithm guarantees the generation of the all negative and positive voltage levels from 0 to $(2^{n+1}-1)V_{in}$. The switching states in this structure are shown in Table 4.

**Table 4** Switching states in the proposed inverter developed from DC source for the positive output voltage levels ($n=2$)

| $v_o$ | $S_1/\overline{S_2}$ | $S_3/\overline{S_4}$ | $S_{5,1}/\overline{S_{6,1}}$ | $S_{5,2}/\overline{S_{6,2}}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| $V_1$ | 1 | 0 | 0 | 0 |
| $2V_1$ | 0 | 1 | 0 | 0 |
| $3V_1$ | 1 | 1 | 0 | 0 |
| $3(V_2-V_1)$ | 0 | 0 | 1 | 0 |
| $2(V_2-V_1)+V_2$ | 1 | 0 | 1 | 0 |
| $2V_2+(V_2-V_1)$ | 0 | 1 | 1 | 0 |
| $3V_2$ | 1 | 1 | 1 | 0 |

In the similar manner to the previous cases, the voltage stress, the current stress and rating of the switches are calculated.

$$(S_1,S_2):\begin{cases}V_{stress}=V_{in}\\ I_{stress}=I_{out}\\ R_s=V_{in}\times I_{out}\end{cases} \quad (24)$$

$$(S_3,S_4):\begin{cases}V_{stress}=V_{in}\\ I_{stress}=2I_{out}\\ R_s=2V_{in}\times I_{out}\end{cases} \quad (25)$$

$$(S_{5,i},S_{6,i}):\begin{cases}V_{stress}=V_{i+1}-V_i\\ I_{stress}=3I_{out}\\ R_s=3(V_{i+1}-V_i)\times I_{out}\end{cases} \quad ,i=1,2,...,(n-1) \quad (26)$$

$$(S_{5,n},S_{6,n}):\begin{cases}V_{stress}=V_n\\ I_{stress}=3I_{out}\\ R_s=3V_n\times I_{out}\end{cases} \quad (27)$$

The characteristics of the proposed multilevel inverters are summarized in Table 5. In this Table, $N_{IGBT}$, $N_{source}$, $N_{level}$ and $G_V$ refer to the number of IGBTs, DC sources, generated voltage levels and voltage gain respectively.

## 3. Comparison

In this section, the implementation of the new topologies developed in this work have been compared to some of the popular multilevel inverters presented in the literature [16, 17, 23-29] to elucidate the advantages being offered through the utilization of the new multilevel inverter topologies. In this comparison the multilevel inverters selected from the literature have been labeled as $R_1-R_4$ [17], $R_5$ [23], $R_6$ [24], $R_7$ [25], $R_8$ [27], $R_9$ [28], $R_{10}-R_{13}$ [16], $R_{14}-R_{17}$ [29], $R_{18}-R_{20}$. [26]; and they have been demonstrated based on the number of generated voltage levels. For the multilevel inverters selected from the literature; the optimal structure ($R_6$ and $R_7$) and the best performance ($R_9$) have been considered as the main criteria for adopting the particular inverter. The characteristics of the inverters from the literature are shown in Table 6.

The comparison of the different multilevel structures is performed in terms of the number of IGBTs, the number of input DC sources, PIV and the rating of the structures that are presented in Fig. 6 (a), (b), (c) and (d) respectively.

The application of the proposed multilevel inverter provides some noticeable benefits. First, it results in reduced number of IGBTs ($P_4$ and $P_5$ along with $R_8$; Fig. 6(a)).

Second, it utilizes lower number of DC sources ( $P_4$ with only one DC source and $P_2$ in other cases; Fig. 6(b)). Third, it reduces the voltage stress level imposed on the switches during operation ( $P_4$, Fig. 6(c)). Fourth, it has less switch rating in comparison to other multilevel inverters ( $P_4$; Fig. 6(d)). The voltage gain of the proposed inverters is another important factor that should be considered. Fig. 6(e) compares the output voltage gain ( $G_V$ ) of the proposed topologies with the other multilevel inverters. According to Fig. 6(e), the application of the new inverter, $P_4$, results in higher output voltage gain. Within Fig. 6, the x-axis ( $N_{level}$ ) has been developed to 100 solely for better illustrating the concept where as it is more common to extend this axis less than that.

Also, it is critical to compare the cost of the proposed inverters to other MLIs from the literature. The cost of the multilevel inverter can be approximated assuming a linear correlation between the overall cost with the number of the major components (e.g. IGBTs, DC voltage sources and transformers). Therefore, to assess the cost associated with the MLI, a simplified cost coefficient ( $G_c$ ) is defined according to (28).

$$G_c = \sum_{i=1}^{N_{IGBT}} a_i + \sum_{j=1}^{N_{source}} b_j + \sum_{l=1}^{N_{transformer}} c_l \quad (28)$$

In (27) $N_{IGBT}$ , $N_{source}$ and $N_{transformer}$ refer to the number of IGBTs, DC sources and transformers; and $a_i$ , $b_j$ and $c_l$ are the cost associated with each component within the MLI structure. Equation (28) can be further simplified assuming an average cost for the similar components used in the MLI structure.

$$G_c = \bar{a}N_{IGBT} + \bar{b}N_{source} + \bar{c}N_{transformer} \quad (29)$$

In (29), $\bar{a}$ , $\bar{b}$ and $\bar{c}$ are the average cost of corresponding components. According to Fig. 6, the application of the proposed structures results in reduced number of IGBTs and switch ratings. Therefore, in the cost analysis, further simplification has been applied to (29) via considering the voltage sources and transformers only.

$$G_c = N_{source} + \left(\frac{\bar{c}}{\bar{b}}\right) N_{transformer} = N_{source} + kN_{transformer} \quad (30)$$

In (30), $k$ is a dimensionless cost coefficient representing the ratio of the average cost of a single transformer to the average cost of a voltage source. A comparative cost analysis has been conducted as a function of $k$ between the MLIs proposed in this work and the ones adopted form the literature ( $R_1 - R_{20}$ ). Fig. 7 and Fig. 8 represent the range of $k$ values that the application of the proposed MLIs would be cost beneficial in comparison to the MLIs selected from the literature.

## 4. Experimental results

Several laboratory-scale prototypes for various topologies of the inverters introduced in this work were designed and built to verify the operation of the proposed inverters (Fig. 9(a)). In this section, from three proposed multilevel inverter with five proposed algorithms ( $P_1 - P_5$ ), 13-level of $P_1$ , 25-level of $P_3$ and 15-level of $P_5$ were chosen. For the prototypes configuration, the BUP306D (with an internal anti-parallel diode, voltage rating of 1200V and current rating of 23A) IGBTs were used as the switching devices and ATMEGA32 AVR microcontroller was used to manipulate all the switches.

For 13-level and 15-level output voltages of the proposed inverters (modulation index of 0.9), VAPD PWM control method with the switching frequency of 5*kHz* was applied [35]. Therefore a PWM voltage waveform for 13 levels of $P_1$ and 15 levels of $P_5$ were generated and the results are shown in Figs. 9(b)-(d) and 10 respectively. It is important to note that, output waveforms are resulted without using any output filters.

The generation of the higher number of voltage levels results in the lower values of THD of the output voltage waveform based on the acceptable THD range determined by the IEEE-519 standard [36]. Accordingly, fundamental frequency switching control strategy with the fundamental frequency of 50*Hz* for the 25-level output voltage was utilized. Following this strategy, a staircase voltage waveform was generated and the results are shown in Fig. 11.

According to Figs. 9-11, the proposed inverters produce an output voltage waveform with 13 levels, 25 levels and 15 levels with maximum output level of 300*V* (by two input voltages of 50*V*), 240*V* (by two input voltages of 20*V*) and 350*V* (by two input voltages of 50*V* and 116*V*). Therefore, voltage gains in these states are 3, 6 and 2.1, respectively.

For 13, 25 and 15 levels of output voltage, the magnitudes of the output and input power is (109.7*W*, 121.57*W*), (162.28*W*, 177.74*W*) and (113.53*W*, 125.31*W*), respectively. As a result, the efficiencies are 90.24%, 91.3% and 90.6% for each case respectively. Table 7 shows the summarized parameters of the proposed inverters in prototypes.

## 5. Conclusion

In this paper, a symmetric and two asymmetric cascaded transformer-based topologies were proposed for multilevel inverters. The basic unit of the inverter was further developed via the addition of low frequency transformers and DC voltage sources and therefore two new flexible MLI structures were proposed. Reduced number of switches and DC sources and low value of PIV and inverter switches' rating besides voltage boosting ability are the main features of the proposed topologies. The application of the proposed algorithms results in producing all the even and odd positive and negative voltage levels, for a given number of DC voltage sources and IGBTs. Also, a simple cost analysis was conducted and the dimensionless cost coefficient was calculated and it was shown that the proposed inverter is capable of decreasing the overall cost of the system if the cost coefficient, $k$ , is selected within the particular range. In order to validate the predicted performance of the inverter, laboratory-scale inverters were designed and assembled and the performance was validated for three different representative cases of 13, 25 and 15 levels of voltage and good agreement was achieved.

**Table 5** The characteristics of the proposed multilevel inverters

| Inverter types | $N_{IGBT}$ | $N_{source}$ | PIV | $R_s$ | Voltage gain ( $G_V$ ), [35] |
|---|---|---|---|---|---|
| $P_1$ | $N_{level}-1$ | $\frac{N_{level}-1}{6}$ | $(N_{level}-1)V_{in}$ | $2(N_{level}-1)\times V_{in}\times I_{out}$ | 3 |
| $P_2$ | $\frac{6\ln(N_{level})}{\ln 7}$ | $\frac{\ln(N_{level})}{\ln 7}$ | $(N_{level}-1)V_{in}$ | $2(N_{level}-1)V_{in}\times I_{out}$ | 3 |
| $P_3$ | $\frac{6\ln(N_{level}+2)-6\ln 3}{\ln 3}$ | $\frac{\ln(N_{level}+2)-\ln 3}{\ln 3}$ | $\frac{6\ln(N_{level}+2)-6\ln 3}{\ln 3}V_{in}$ | $2(N_{level}-1)V_{in}\times I_{out}$ | $\frac{(N_{level}-1)\ln 3}{2(\ln(N_{level}+2)-\ln 3)}$ |
| $P_4$ | $\frac{2\ln(N_{level}+1)}{\ln 2}$ | 1 | $\frac{2\ln(N_{level}+1)}{\ln 2}V_{in}$ | $2(N_{level}-3)V_{in}\times I_{out}$ | $\frac{N_{level}-1}{2}$ |
| $P_5$ | $\frac{2\ln(N_{level}+1)}{\ln 2}$ | $\frac{\ln(N_{level}+1)-2\ln 2}{\ln 2}$ | $\frac{4N_{level}-10}{3}V_{in}$ | $3(N_{level}-3)V_{in}\times I_{out}$ | $\frac{3(N_{level}-1)\ln 2}{2(N_{level}-1)\ln 2-2\ln(N_{level}+1)}$ |

**Table 6** The characteristics of the proposed multilevel inverters

| Types | $N_{IGBT}$ | $N_{source}$ | $PIV$ | $R_s$ | Voltage Gain ( $G_V$ ) |
|---|---|---|---|---|---|
| $R_1$ , [17] | $2(N_{level}-1)$ | $\frac{(N_{level}-1)}{2}$ | $2(N_{level}-1)V_{dc}$ | $2(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_2$ , [17] | $4(\frac{\ln(N_{level}+1)}{\ln 2}-1)$ | $(\frac{\ln(N_{level}+1)}{\ln 2}-1)$ | $2(N_{level}-1)V_{dc}$ | $2(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_3$ , [17] | $4(\frac{\ln(\frac{N_{level}-1}{2})}{\ln 3}+1)$ | $(\frac{\ln(\frac{N_{level}-1}{2})}{\ln 3}+1)$ | $2(N_{level}-1)V_{dc}$ | $2(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_4$ , [17] | $\frac{4\ln N_{level}}{\ln 3}$ | $\frac{\ln N_{level}}{\ln 3}$ | $2(N_{level}-1)V_{dc}$ | $2(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_5$ , [23] | $2(N_{level}-1)$ | $(N_{level}-1)$ | $2(N_{level}-1)V_{dc}$ | $2(N_{level}-1)V_{dc}I_{out}$ | $\frac{1}{2}$ |
| $R_6$ , [24] | $\ln(N_{level})\times\frac{8}{\ln 5}$ | $\frac{\ln(N_{level})}{\ln 3}$ | $\frac{3}{2}(N_{level}-1)V_{dc}$ | $\frac{3}{2}(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_7$ , [25] | $\frac{6\ln(N_{level})}{\ln(5)}$ | $\frac{2\ln(N_{level})}{\ln(5)}$ | $\frac{5}{4}(N_{level}-1)V_{dc}$ | $\frac{5}{4}(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_8$ , [27] | $\frac{2\ln(N_{level}+1)}{\ln(2)}$ | $\frac{\ln(N_{level}+1)}{\ln(2)}-1$ | $12(5^{\frac{1}{2}(\frac{\ln(N_{level}+1)}{\ln 2}-3)})V_{dc}$ | $12(5^{\frac{1}{2}(\frac{\ln(N_{level}+1)}{\ln 2}-3)})V_{dc}I_{out}$ | $\frac{4\times 5^{\frac{1}{2}(\frac{\ln(N_{level}+1)}{\ln(2)}-3)}}{5^{\frac{1}{2}(\frac{\ln(N_{level}+1)}{\ln(2)}-1)}}-1$ |
| $R_9$ , [28] | $\frac{6\ln N_{level}}{\ln(7)}$ | $\frac{2\ln N_{level}}{\ln(7)}$ | $2(N_{level}-1)V_{dc}$ | $2(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_{10}$ , [16] | $\frac{5}{6}(N_{level}-3)+6$ | $\frac{1}{2}(N_{level}-3)+1$ | $(\frac{7}{2}(N_{level}-3)+6)V_{dc}$ | $(\frac{7}{2}(N_{level}-3)+6)V_{dc}I_{out}$ | 1 |
| $R_{11}$ , [16] | $\frac{5}{12}(N_{level}+3)+6$ | $\frac{1}{4}(N_{level}+3)+1$ | $(\frac{10}{3}(N_{level}+3)-13)V_{dc}$ | $(\frac{10}{3}(N_{level}+3)-13)V_{dc}I_{out}$ | 1 |
| $R_{12}$ , [16] | $\frac{5\ln(\frac{N_{level}-4}{5})}{\ln(3)}+11$ | $\frac{3\ln(\frac{N_{level}-4}{5})}{\ln(3)}+4$ | $(\frac{82N_{level}-263}{5})V_{dc}$ | $(\frac{82N_{level}-363}{5})V_{dc}I_{out}$ | 1 |
| $R_{13}$ , [16] | $\frac{5\ln(N_{level}+5)}{\ln(2)}-9$ | $\frac{3\ln(N_{level}+5)}{\ln(2)}-8$ | $(\frac{7N_{level}-9}{2})V_{dc}$ | $(\frac{7N_{level}-9}{2})V_{dc}I_{out}$ | 1 |
| $R_{14}$ , [29] | $\frac{3}{2}(N_{level}-1)$ | $\frac{1}{2}(N_{level}-1)$ | $\frac{5}{2}(N_{level}-1)V_{dc}$ | $\frac{5}{2}(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_{15}$ , [29] | $\frac{6\ln N_{level}}{\ln 5}$ | $\frac{2\ln N_{level}}{\ln 5}$ | $\frac{5}{2}(N_{level}-1)V_{dc}$ | $\frac{5}{2}(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_{16}$ , [29] | $3(\frac{\ln(N_{level}+1)}{\ln 2}-1)$ | $(\frac{\ln(N_{level}+1)}{\ln 2}-1)$ | $\frac{16}{3}(\frac{N_{level}-1}{2})V_{dc}$ | $\frac{16}{3}(\frac{N_{level}-1}{2})V_{dc}I_{out}$ | 1 |
| $R_{17}$ , [29] | $\frac{6\ln N_{level}}{\ln 7}$ | $\frac{2\ln N_{level}}{\ln 7}$ | $\frac{8}{3}(N_{level}-1)V_{dc}$ | $\frac{8}{3}(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_{18}$ , [26] | $N_{level}+3$ | $\frac{1}{2}(N_{level}-1)$ | $3(N_{level}-1)V_{dc}$ | $3(N_{level}-1)V_{dc}I_{out}$ | 1 |
| $R_{19}$ , [26] | $\frac{2\ln[2(N_{level}+1)]}{\ln 2}$ | $\frac{\ln(N_{level}+1)}{\ln 2}-1$ | $3(N_{level}-1)V_{dc}$ | $3(N_{level}-1)V_{dc}I_{out}$ | 1 |

| | | | | | |
|---|---|---|---|---|---|
| $R_{20}$ , [26] | $\frac{N_{level}+9}{2}$ | $\frac{N_{level}+1}{4}$ | $3(N_{level}-1)V_{dc}$ | $3(N_{level}-1)V_{dc}I_{out}$ | 1 |

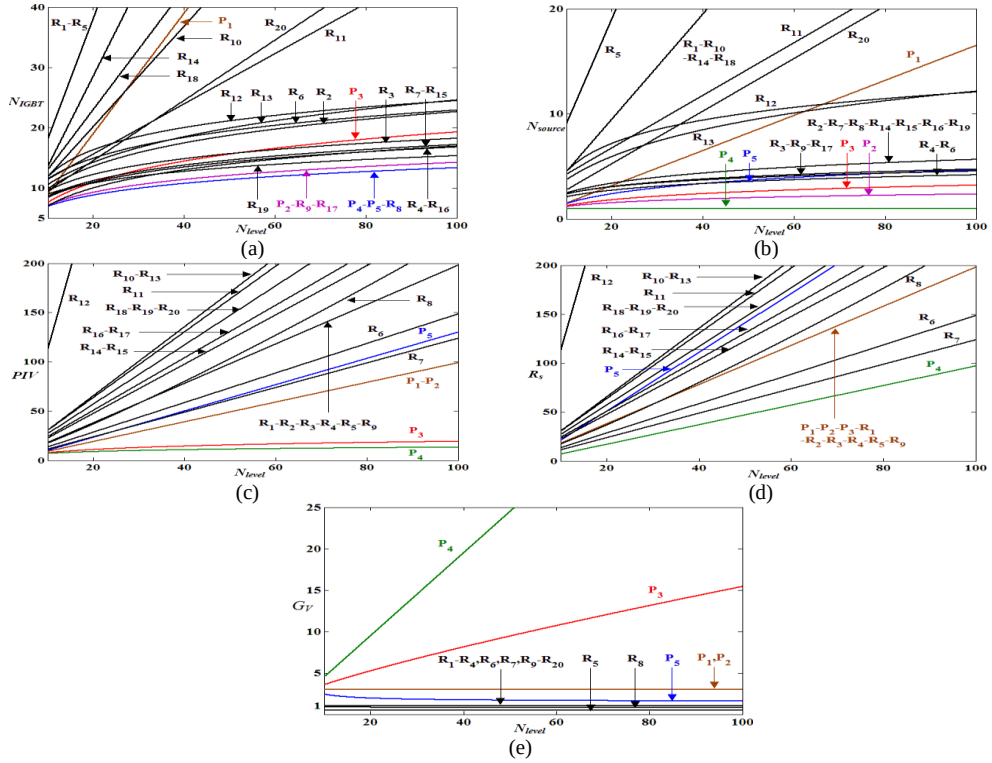


***Fig. 6.*** *Comparison among the different components of the proposed inverter with the inverters adopted from the literature*
***(a)*** variation of $N_{IGBT}$ versus $N_{level}$ , ***(b)*** variation of $N_{source}$ versus $N_{level}$ ,***(c)*** variation of PIV versus $N_{level}$ , ***(d)*** variation of $R_s$ versus $N_{level}$ **(e)** comparison of $G_V$ versus $N_{level}$

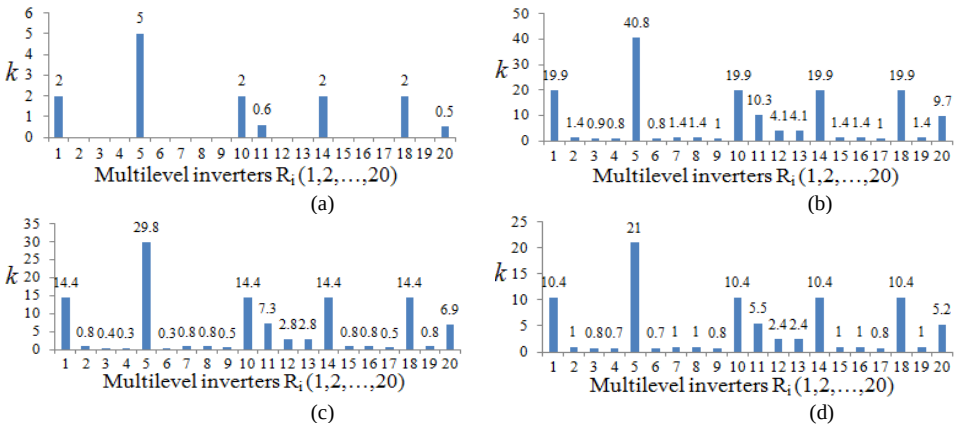


**Fig. 7.** *Variation of $G_c$ for different values of $k$*

***(a)*** proposed inverter $P_1$ , ***(b)*** proposed inverter $P_2$ ,***(c)*** proposed inverter $P_3$ ,***(d)*** proposed inverter $P_4$

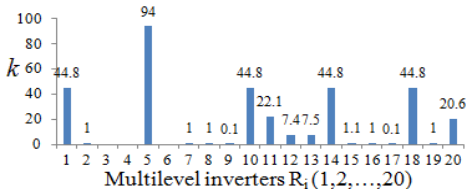


**Fig. 8.** *Variation of $G_c$ for different values of $k$ for proposed inverter $P_5$*

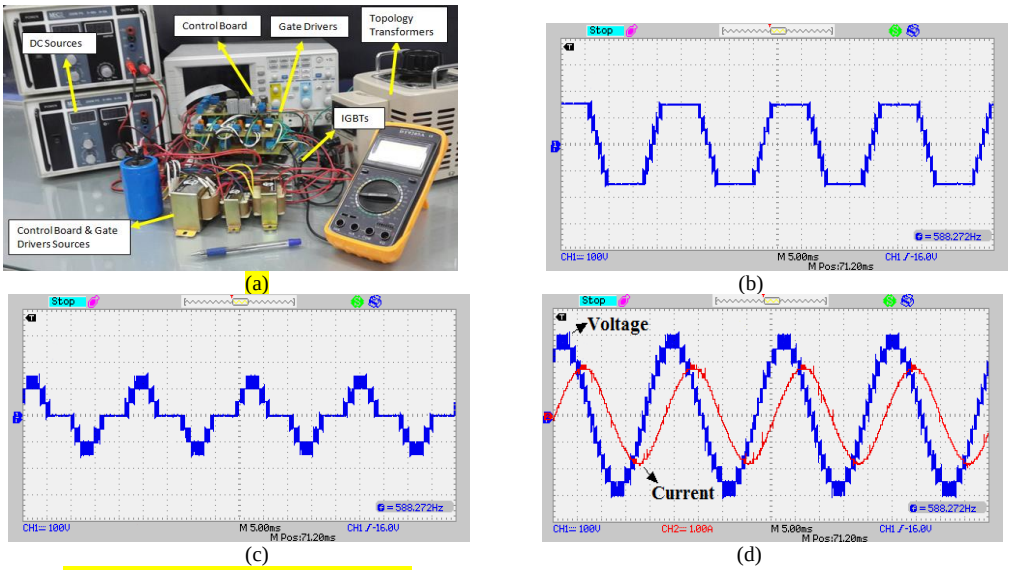


**Fig. 9.** (a) *Prototype of the proposed inverters; Output voltage levels in 13-level of $P_1$ with 0.45 power factor (69Ω and 490mH),* ***(b)*** Output voltage of first module, ***(c)*** Output voltage of second module,***(d)*** Output voltage and current of inverter

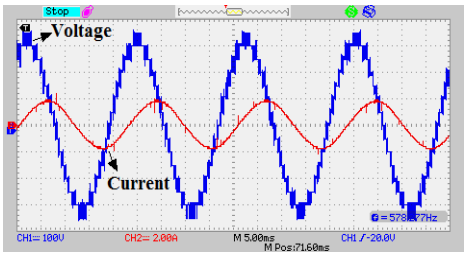


**Fig. 10.** *Output voltage levels of inverter in 15-level of $P_5$ with 0.4 power factor (72Ω and 590mH)*

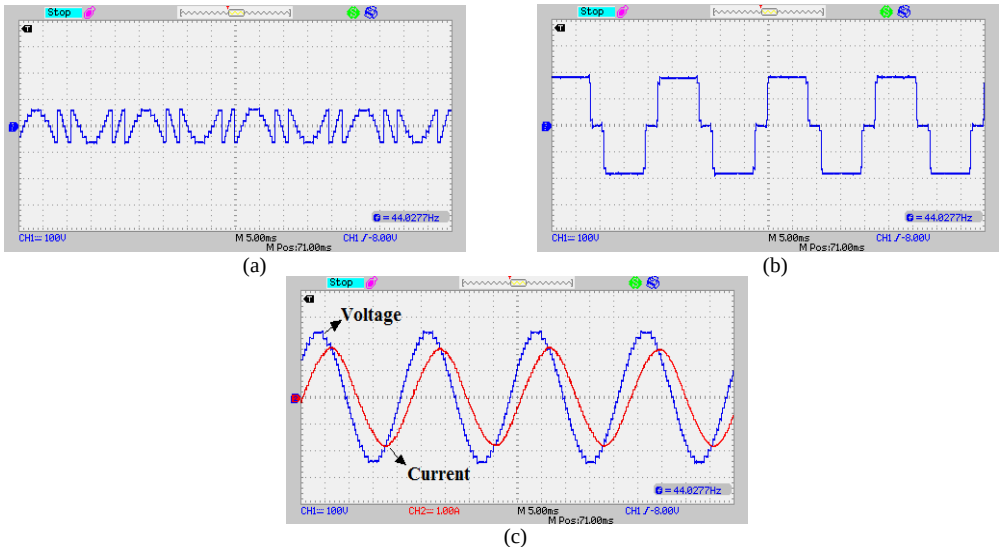


**Fig. 11.** *Output voltage levels and current in 25-level of $P_5$ with 0.75 power factor (101Ω and 322mH)*
***(a)*** Output voltage of first module, ***(b)*** Output voltage of second module,***(c)*** Output voltage and current of inverter

**Table 7** Summarized parameters of proposed inverters in laboratory prototypes

| Inverter types | Control method | Input voltage [V] | Output voltage[V] | Voltage gaim | Transformer turn ratio | THD (%) |
|---|---|---|---|---|---|---|
| 13 level of P1 | PWM | 50, 50 | 300 | 3 | 2:1, 2:1 | 9.16 |
| 25 level of P3 | fundamental frequency switching | 20, 20 | 240 | 6 | 2:1, 8:1 | 3.43 |
| 15 level of P5 | PWM | 50, 116 | 350 | 2.1 | 2:1 | 7.64 |

## 6. References


7. [1] Khan, F. A., Pal, N., Saeed, S. H.: 'Review of solar photovoltaic and wind hybrid energy systems for sizing strategies optimization techniques and cost analysis methodologies', Renewable and Sustainable Energy Reviews, 2018, 92, pp. 937-947
8. [2] Rajbongshi, R., Borgohain, D., Mahapatra, S.: ' Optimization of PV-biomass-diesel and grid base hybrid energy systems for rural electrification by using HOMER', Energy, 2017, 126, 461-474
9. [3] Yu, J., Dou, C., Li, X.: 'MAS-Based Energy Management Strategies for a Hybrid Energy Generation System', IEEE Trans. Ind. Electron., 2016, 63, (6), pp. 3756- 3764
10. [4] Guggenberger, J. D., Elmore, A. C., Tichenor, J. L., Crow, M. L.: 'Performance Prediction of a Vanadium Redox Battery for Use in Portable, Scalable Microgrids', IEEE Trans. Smart Grid., 2012, 3, (4), pp. 2109-2116
11. [5] Nabae, A., Takahashi, I., Akagi, H.: 'A new neutral-point-clamped PWM inverter', IEEE Trans. industry applications, 1981, (5), pp. 518-523.
12. [6] Saeidabadi, S., Ashraf Gandomi, A., Hosseini, S.H., Sabahi, M., Ashraf Gandomi, Y.: 'New improved three-phase hybrid multilevel inverter with reduced number of components', IET Power Electron., 2017, 10, (12), pp.1403-1412
13. [7] Agrawal, R. and Jain, S.: 'Multilevel inverter for interfacing renewable energy sources with low/medium-and high-voltage grids', IET Renewable Power Gen., 2017, 11, (14), pp.1822-1831.
14. [8] Umesh, B. S., Sivakumar, K.: 'Multilevel Inverter Scheme for Performance Improvement of Pole-Phase-Modulated Multiphase Induction Motor Drive', IEEE Trans. Ind. Electron, 2016, 63, (4), pp. 2036-2043
15. [9] Khomfoi, S., Tolbert, L. M.: 'Multilevel power converters', Power electronics handbook,2007, pp. 451-482
16. [10] Marchesoni, M., Tenca, P.: 'Diode-clamped multilevel converters: a practicable way to balance DC-link voltages', IEEE Trans. Ind. Electron., 2002, 49, (4), pp. 752-765

17. [11] Ashraf Gandomi, A., Varesi, K., Hosseini, S. H.: 'Control strategy applied on double flying capacitor multi-cell inverter for increasing number of generated voltage levels', IET Power Electron., 2015, 8, (6), pp. 887-897
18. [12] Peng, F. Z.: 'A generalized multilevel inverter topology with self voltage balancing', IEEE Trans. Ind. 2001, 37, (2), pp. 611–618
19. [13] Nami, A., Zare, F., Ghosh, A., Blaabjerg, F.: 'A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode clamped h-bridge cells', IEEE Trans. Power Electron., 2011, 26, (1), pp. 51–65
20. [14] Amini, J., Viki, A. H., Radan, A., Moallem, M.: 'A General Active Capacitor Voltage Regulating Method for L-Level M-Cell N-Phase Flying Capacitor Multilevel Inverter With Arbitrary DC Voltage Distribution', IEEE Trans. Ind. Electron, 2016, 63, (5), pp. 2659-2668
21. [15] Malinowski, M., Gopakumar, K., Rodriguez, J., Perez, M. A.: 'A survey on cascaded multilevel inverters', IEEE Trans. Ind. Electron., 2010, 57, (7), pp. 2197–2206
22. [16] Babaei, E., Laali, S., Bayat, Z.: 'A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches', IEEE Trans. Ind. Electron., 2015, 62, (2), pp. 922-929
23. [17] Lai, Y. S., Shyu, F. S.: 'Topology for hybrid multilevel inverter', IEEE Proceedings Electric Power Applications, 2002, 149, (6), pp. 449-458
24. [18] Oskuee, M. R. J., Karimi, M., Ravadanegh, S. N., Gharehpetian, G. B.: 'An Innovative Scheme of Symmetric Multilevel Voltage Source Inverter With Lower Number of Circuit Devices', IEEE Trans. Ind. Electron., 2015, 62, (11), pp. 6965-6973
25. [19] Gupta, K. K., Jain, S.: 'A Novel Multilevel Inverter Based on Switched DC Sources', IEEE Trans. Ind. Electron., 2014, 61, (7), pp. 3269-3278
26. [20] Najafi, E., Yatim, A. H. M.: 'Design and Implementation of a New Multilevel Inverter Topology', IEEE Trans. Ind. Electron., 2012, 59, (11), pp. 4148-4154
27. [21] Kangarlu, M. F., Babaei, E., Laali, S.: 'Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources', IET Power Electron., 2012, 5, (5), pp. 571-581
28. [22] Chattopadhyay, S. K., Chakraborty, C.: 'A New Multilevel Inverter Topology With Self-Balancing Level Doubling Network', IEEE Trans. Ind. Electron., 2014, 61, (9), pp. 4622-4631
29. [23] Waltrich, G., Barbi, I.: 'Three-phase cascaded multilevel inverter using power cells with two inverter legs in series', IEEE Trans. Ind. Appl., 2010, 57, (8), pp. 2605-2612
30. [24] Ebrahimi, J., Babaei, E., Gharehpetian, G. B.: 'A New Multilevel Converter Topology With Reduced Number of Power Electronic Components', IEEE Trans. Ind. Electron., 2012, 59, (2), pp. 655-667
31. [25] Shalchi Alishah, R., Nazarpour, D., Hosseini, S. H., Sabahi, M.: 'Reduction of Power Electronic Elements in Multilevel Converters Using a New Cascade Structure', IEEE Trans. Ind. Electron., 2015, 62, (1), pp. 256-269
32. [26] Babaei, E., Hosseini, S.H.: 'New cascaded multilevel inverter topology with minimum number of switches', Elsevier Journal of Ene. Conv and Man., 2009, 50, (11), pp. 2761-2767
33. [27] Babaei, E., Alilu, S., Laali, S.: 'A New General Topology for Cascaded Multilevel Inverters With Reduced Number of Components Based on Developed H-Bridge', IEEE Trans. Ind. Electron., 2014, 61, (8), pp. 3932-3939
34. [28] Babaei, E., Laali S., Alilu, S.: 'Cascaded Multilevel Inverter With Series Connection of Novel H-Bridge Basic Units', IEEE Trans. Ind. Electron., 2014, 61, (12), pp. 6664-6671
35. [29] Mokhberdoran, A., Ajami, A.: 'Symmetric and Asymmetric Design and Implementation of New Cascaded Multilevel Inverter Topology', IEEE Trans. Power Electron., 2014, 29, (12), pp. 6712-6724
36. [30] Li, Z., Wang, P., Li, Y., Gao, F.: 'A Novel Single-Phase Five-Level Inverter With Coupled Inductors', IEEE Trans. Power Electron., 2012, 27, (6), pp. 2716–2725
37. [31] Banaei, M. R., Khounjahan H., Salary, E.: 'Single-source cascaded transformers multilevel inverter with reduced number of switches', IET Power Electron., 2012, 5, (9), pp. 1748-175
38. [32] Tan, C., Xiao, D., Fletcher J. E., Rahman, M. F.: 'Carrier-Based PWM Methods With Common-Mode Voltage Reduction for Five-Phase Coupled Inductor Inverter', IEEE Trans. Ind. Electron., 2016, 63, (1), pp. 526-537
39. [33] Sharifzade, M., Vahedi, H., Portillo, R., Khenar, M., Sheikholeslami, A., Franquelo, L., Al-Haddad, K.: 'Hybrid SHM-SHE Pulse Amplitude Modulation for High Power Four-Leg Inverter"' IEEE Trans. Ind. Electron, 2016, 63, 11, pp. 7234-7242
40. [34] Lee, S. S., Chu, B., Idris, N. R. N., Goh H. H., Heng, Y. E.: 'Switched-Battery Boost-Multilevel Inverter with GA Optimized SHEPWM for Standalone Application', IEEE Trans. Ind. Electron., 2016, 63, (4), pp. 2133-2142
41. [35] Ashraf Gandomi, A., Saeidabadi, S., Hosseini, S. H., Babaei, E., Sabahi, M.: 'Transformer-based inverter with reduced number of switches for renewable energy applications', IET Power Electron., 2015, 8, (10), pp. 1875-1884
42. [36] Std. 519-1992: 'IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems', 1992.